

Amendments To the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 Claim 27 (currently amended): A processing core of a processing system for processing
2 information using hardware-assisted context switching, comprising;
3 a processing unit;
4 an instruction cache for storing instructions for non-time-critical tasks and a
5 code random access memory for storing instructions required for causing serving of time-
6 critical tasks, the instruction cache and the code random access memory coupled to the
7 processing unit;
8 a register group for updating status of registers related to time critical tasks;
9 and
10 another register group coupled to the processing unit[;],
11 [a data memory and another data memory coupled to the processing unit; and
12 a low priority interrupt controller and a high priority interrupt controller
13 coupled to the processing unit; and
14 wherein the instruction cache, the register group, the data memory, and the low
15 priority interrupt controller are dedicated to performing non-time-critical tasks by the
16 processing unit; and
17 wherein the code random access memory, the another register group, the
18 another data memory, and the high priority interrupt controller are dedicated to performing
19 time-critical tasks by the processing unit]
20 wherein the processing unit need access status of registers only in the register
21 group for execution of time-critical tasks thereby avoiding saving and restoring
22 status of the another registers for execution of time-critical tasks.

1 Claim 28 (previously presented): The processing core according to Claim 27, wherein one
2 of the time-critical tasks is providing additional data to a video engine unit during a video
3 compression process.

1 Claim 29 (previously presented): The processing core according to Claim 28, wherein the
2 additional data is provided to the video engine unit within a time interval of less than two
3 microseconds.

1 Claim 30 (previously presented): The processing core according to Claim 27, wherein one
2 of the non-time-critical tasks is multiplexing of audio and video streams.

1 Claim 31 (previously presented): The processing core according to Claim 27, wherein one
2 of the one-time-critical tasks is demultiplexing Motion Picture Expert Group (MPEG)
3 streams.

1 Claim 32 (previously presented): The processing core according to Claim 27, wherein the
2 non-time-critical tasks are user interface application.

1 Claim 33 (previously presented): The processing core according to Claim 32, wherein one
2 of the user interface applications is providing an on-screen display every two seconds.

1 Claim 34 (currently amended): A method of processing information by a processing core
2 for a processing system, comprising:
3 providing a processing unit;
4 coupling an instruction cache and a code random access memory to the
5 processing unit;
6 coupling a register group and another register group to the processing unit;
7 coupling a data memory and another data memory to the processing unit;
8 coupling a low priority interrupt controller and a high priority interrupt controller
9 to the processing unit;

performing non-time-critical tasks through dedicated use by the processing unit of the instruction cache, the register group, the data memory, and the low priority interrupt controller; [and]

performing time-critical tasks through dedicated use by the processing unit of the code random access memory, the another register group, the another data memory, and the high priority interrupt controller; and

accessing status of registers only in the register group for execution of time-critical tasks thereby avoiding saving and restoring status of the another registers for execution of time-critical tasks.

Claim 35 (previously presented): The method according to Claim 34, wherein performing time-critical tasks further comprises providing additional data to a video engine unit during a video compression process.

Claim 36 (previously presented): The method according to Claim 35, wherein providing additional data further comprises providing the additional data to the video engine unit within a time interval of less than two microseconds.

Claim 37 (previously presented): The method according to Claim 34, wherein performing non-time-critical tasks further comprises multiplexing of audio and video streams.

Claim 38 (previously presented): The method according to Claim 34, wherein performing non-time-critical tasks further comprises demultiplexing Motion Picture Expert Group (MPEG) streams.

Claim 39 (previously presented): The method according to Claim 34, wherein performing non-time-critical tasks further comprises performing user interface applications.

1 Claim 40 (previously presented): The method according to Claim 39, wherein performing
2 user interface applications further comprises providing an on-screen display every two
3 seconds.

1 Claim 41 (currently amended): An audio and video encoder/decoder, comprising:

2 a processing system;

3 a video engine unit and a video interface unit both coupled to the processing
4 system;

5 an audio engine unit and an audio interface unit both coupled to the processing
6 system and

7 wherein the processing system has a processing core that includes:

8 a processing unit;

9 an instruction cache for storing instructions for non-time-critical tasks and a
10 code random access memory for storing instructions required for causing serving of time-
11 critical tasks, the instruction cache and the code random access memory coupled to the
12 processing unit;

13 a register group for updating status of registers related to time critical tasks;

14 and

15 another register group coupled to the processing unit;

16 a data memory and another data memory coupled to the processing unit;

17 and

18 [a low priority interrupt controller and a high priority interrupt controller
19 coupled to the processing unit; and

20 wherein the instruction cache, the register group, the data memory, and the low
21 priority interrupt controller are dedicated to performing non-time-critical tasks by the
22 processing unit; and

23 wherein the code random access memory, the another register group, the
24 another data memory, and the high priority interrupt controller are dedicated to performing
25 time-critical tasks by the processing unit]

26 wherein the processing unit need access status of registers only in the register
 27 group for execution of time-critical tasks thereby avoiding saving and restoring status of
 28 the another registers for execution of time-critical tasks.

1 Claim 42 (previously presented): The audio and video encoder/decoder according to
 2 Claim 41, wherein one of the time-critical tasks is providing additional data to a video
 3 engine unit during a video compression process.

1 Claim 43 (previously presented): The audio and video encoder/decoder according to
 2 Claim 42, wherein the additional data is provided to the video engine unit within a time
 3 interval of less than two microseconds.

1 Claim 44 (previously presented): The audio and video encoder/decoder according to
 2 Claim 41, wherein one of the non-time critical tasks is multiplexing of audio and video
 3 streams.

1 Claim 45 (previously presented): The audio and video encoder/decoder according to
 2 Claim 41, wherein one of the non-time-critical tasks is demultiplexing Motion Picture
 3 Expert Group (MPEG) streams.

1 Claim 46 (previously presented): The audio and video encoder/decoder according to
 2 Claim 41, wherein the non-time-critical tasks are user interface applications.

1 Claim 47 (previously presented): The audio and video encoder/decoder according to
 2 Claim 46, wherein one of the user interface applications is providing an on-screen display
 3 every two seconds.